# CERTIFICATION OF TRANSLATION

I, Jeonghee Lee, an employee of Y.P.LEE, MOCK & PARTNERS of The Cheonghwa Bldg., 1571-18 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statements in the English language in the attached translation of the priority document (Korean Patent Application No. 02-12563), consisting of 22 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 28 day of January, 2005

Jeonghee Lee

Jeonghee Lee

# ABSTRACT

[Abstract of the Disclosure]

A ferroelectric memory device using a via etch blocking layer and a method for fabricating the same are provided. The ferroelectric memory device includes a plurality of ferroelectric capacitors disposed two-dimensionally on a lower interlayer insulating layer in the line direction and the column direction. The tops of the ferroelectric capacitors are exposed through an interlayer insulating layer covering between the ferroelectric capacitors. A via etch blocking layer pattern is formed only on the interlayer insulating layer. A plurality of plate lines each is electrically connected to the ferroelectric capacitors on at least two neighboring lines and contact the via etch blocking layer pattern between the ferroelectric capacitors. Accordingly, high integration is achieved since a via hole is not required in each cell for connection of plate lines. Further, the lower interlayer insulating layer is protected by the via etch blocking layer pattern, preventing the capacitor characteristics from being degraded.

[Representative Drawing]

FIG. 9.

# SPECIFICATION

[Title of the Invention]

FERROELECTRIC MEMORY DEVICE USING VIA ETCH BLOCKING LAYER AND METHOD FOR FABRICATING THE SAME

[Brief Description of the Drawings]

FIGS. 1 through 9 are cross-sectional views of a ferroelectric memory device and a method for fabricating the same according to an embodiment of the present invention.

<Explanation of Reference Numerals Designating the Major Elements of the Drawings>

20: 1st lower interlayer insulating layer

35: 2nd lower interlayer insulating layer

60: Ferroelectric capacitor

70: Interlayer insulating layer

80: Via etch blocking layer pattern

90: Encapsulated barrier layer

95: 1st upper interlayer insulating layer

105a: Main word line

110: 2nd upper interlayer insulating layer

115: Slit-shaped common via hole

120: Plate line

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a semiconductor device, and more particularly, to a ferroelectric memory device including a ferroelectric capacitor and a method for fabricating the same.

Recently, ferroelectric memory devices using a ferroelectric layer have been recognized as the memory devices for the next generation. The ferroelectric memory device works by controlling the direction of polarization according to the direction of an applied electric field, and a digital 0 or 1 is stored according to the direction of remnant polarization when the electric field is removed. This kind of ferroelectric memory device is characterized by high endurance, high speed of tens of nanoseconds, low driving voltage of less than 5V and low power dissipation. However, the ferroelectric memory device must be more integrated to be used as a memory product, besides the characteristics.

To achieve high integration of the ferroelectric memory device, it is necessary not only to embody the cell structure of 1T/1C (1 transistor/1 ferroelectric capacitor), miniaturize the ferroelectric capacitor, and develop multiple wiring processes, but also to guarantee hot temperature retention, and powerful writing and reading abilities compared to DRAM and SRAM.

Especially, miniaturization of the ferroelectric capacitor becomes the most important and complicated technology as high integration technology progresses. This is because changes of the ferroelectricity have not yet been fully verified according to ferroelectric capacitor regions obviously reduced by the high integration, and subsequent processes for the reduced capacitors have become more difficult. In addition, via holes in each cell need to be connected to plate lines according to the characteristics of the ferroelectric memory device. The conventional method for fabricating via holes in each cell is not available in a capacitor region with a design rule less than 0.25μm.

Therefore, there is a need for new technology for forming via holes to be connected to plate lines in a reduced capacitor. This technology should not damage the capacitor. In general, a damage might occur due to etching chemicals (gas or solution), and this can degrade the capacitor by degrading the remnant polarization or its distribution. Especially, if the distribution of remnant polarization in each capacitor is irregular, it reduces the sensing margin in a ferroelectric memory device. This is because the process method of a ferroelectric memory device is based on comparing the remnant polarization of both a reference cell capacitor and a memory cell capacitor and recognizing the difference between them.

[Technical Goal of the Invention]

It is an object of the present invention to provide a more integrated ferroelectric memory device, by improving the connection between plate lines and a ferroelectric capacitor.

It is another object of the present invention to provide a method for fabricating a ferroelectric memory device including methods for forming via holes in fabricating a highly integrated ferroelectric memory device, without any problems relating to degrading the characteristic of a capacitor.

[Structure and Operation of the Invention]

To accomplish the object of the present invention, a ferroelectric memory device comprises a plurality of ferroelectric capacitors disposed two-dimensionally

on a lower interlayer insulating layer formed on a semiconductor substrate in the line direction and the column direction. The tops of the ferroelectric capacitors are exposed through an interlayer insulating layer covering between the ferroelectric capacitors. A via etch blocking layer pattern is formed only on the interlayer insulating layer. An upper interlayer insulating layer is formed on the via etch blocking layer pattern. A plurality of plate lines each is electrically connected to the ferroelectric capacitors on at least two neighboring lines and contact the via etch blocking layer between the ferroelectric capacitors.

The via etch blocking layer and the interlayer insulating layer are made of materials of different etch selectivity. For example, if the upper interlayer insulating layer is made of an oxide layer, and the via etch stop layer is made of a titanium oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

An encapsulated barrier layer is clad on the via etch blocking layer pattern and deters permeation of hydrogen. The encapsulated barrier layer is made of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer, or a cesium oxide layer.

On the while, the ferroelectric capacitors include a lower electrode, a ferroelectric layer pattern, and an upper electrode layer sequentially, and the plate lines directly contact the upper electrodes on at least two neighboring lines. At this time, the plate lines are common plate lines which directly contact the upper electrodes on at least two neighboring lines through a slit-shaped common via hole passing through the upper interlayer insulating layer.

To accomplish another object of the present invention, a method for fabricating a ferroelectric memory device comprises forming a lower interlayer insulating layer on a semiconductor substrate. A plurality of ferroelectric capacitors are formed two-dimensionally on the lower interlayer insulating layer, in the line direction and the column direction. An interlayer insulating layer covering the ferroelectric capacitors and a via etch blocking layer are sequentially formed. The via etch blocking layer and the interlayer insulating layer are patterned to form cell via holes which expose the tops of the ferroelectric capacitors. A 1$^{st}$ upper interlayer insulating layer is formed to completely fill the cell via holes. Main wordlines are formed on a top of the 1$^{st}$ upper interlayer insulating layer. A 2$^{nd}$ upper interlayer insulating layer is formed to entirely cover the main wordlines. A plurality of plate lines are formed to each electrically access the ferroelectric

capacitors on at least two neighboring lines and contact the via etch blocking layer pattern between the ferroelectric capacitors by etching the 2nd upper interlayer insulating layer and the 1st upper interlayer insulating layer using the patterned via etch blocking layer as an etch finishing point and depositing a conductive layer.

The via etch blocking layer and the interlayer insulating layer are made of materials of different etch selectivity. The upper interlayer insulating layer is made of an oxide layer, and the via etch blocking layer is made of a titanium oxide layer, a silicon nitride layer, or a silicon oxynitride layer.

The forming of the ferroelectric capacitors comprises sequentially forming a lower electrode layer, a ferroelectric layer and an upper electrode layer on the lower interlayer insulating layer; and patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer continuously to form a plurality of ferroelectric layers in which the lower electrode, the ferroelectric layer pattern and the upper electrode are layered sequentially.

The plate lines are common plate lines that directly contact the ferroelectric capacitors on at least the two neighboring lines through a slit-shaped common via hole penetrating the 1st and 2nd upper interlayer insulating layers.

According to the present invention, since plate lines and capacitors are connected through a slit-shaped common via hole, elements restricting integration are removed in forming via holes for the connection of plate lines in each cell. In addition, a via etch blocking layer is used as an etch finish point, thus preventing damage to the lower interlayer insulating layer. This overcomes the conventional problem in that a capacitor characteristic is degraded by permeation of etching chemicals into a dielectric layer.

The present invention now will be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete and, will fully convey the concept of the present invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or a substrate, it can be directly on the other layer or the substrate, or interlayer layers

may also be present. In drawings, the same reference numerals represent the same element.

FIG. 9 shows a sectional view of a ferroelectric memory device according to an embodiment of the present invention. According to the present invention, cell transistors are disposed two-dimensionally on the semiconductor substrate in the line direction and the column direction. FIG. 9 shows a sectional view cut along a column perpendicular to the line direction of an extension of the gate of each cell transistor.

Referring to FIG. 9, a plurality of cell transistors are formed on the semiconductor substrate 10 of which an isolation process is completed. A cell transistor includes a gate 15, a source region 17 and a drain region 18 at both sides of the gate 15. A contact pad 25 is formed on top of a source region 17 and a drain region 18. A bit line 30 is electrically connected to the drain region 18 of the cell transistors passing through the 1st lower interlayer insulating layer 20 by the contact pad 25. A 2nd lower interlayer insulating layer 35 is also formed and contact plugs 40 are formed on top of the drain region 18 passing through the 2nd lower interlayer insulating layer 35 and the 1st lower interlayer insulating layer 20. The contact plugs 40 are electrically connected to the source regions 17 of the cell transistors by the contact pads 25. The contact pads 25 are formed when the aspect ratio of each contact hole for forming the bit line 30 and the contact plug 40, is large, and thus, are sometimes omitted.

On top of the contact pads 25 are formed the ferroelectric capacitors 60. The cell transistors and contact plugs 40 are two-dimensionally disposed, and consequently, the ferroelectric capacitors 60 are also two-dimensionally disposed.

Each ferroelectric capacitor 60 includes a lower electrode 45, a ferroelectric layer pattern 50 and an upper electrode 55, layered sequentially. The lower electrode 45 is located on top of the contact plug 40 and is electrically connected to the source region 17 through the contact plug 40. Further, the lower electrode 45 consists of multiple layers including an adhesive layer, a lower diffusion barrier layer, a lower metallic oxide layer and a lower metallic layer. The total thickness of the lower electrode can range from 1000 to 3000 Å. The lower diffusion barrier layer is formed to prevent oxygen from diffusing. The ferroelectric layer pattern 50 is made of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer or $SrBi(Ta, Nb)_2O_9$. The upper electrode 55 can be a dual layer of an upper metallic oxide layer and an upper diffusion barrier

layer. The total thickness of the upper electrode can also range from 1000 to 3000 Å. The upper electrode 55 and the lower electrode 45 are made of a metal such as Pt, Ir, Ru, Rh, etc. Accordingly, their metallic oxides such as $IrO_2$, $RhO_2$ or $RuO_2$ also can be used for the upper electrode 55 and the lower electrode 45.

The upper electrode 55 of the ferroelectric capacitor 60 is exposed by the interlayer insulating layer 70 which covers the regions between the ferroelectric capacitors 60. The via etch blocking layer pattern 80 is made only on the interlayer insulating layer 70. On top of the via etch blocking layer is clad an encapsulated barrier layer 90. The encapsulated barrier layer 90 can be a metallic oxide layer such as an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer or a cesium oxide layer.

This kind of encapsulated barrier layer 90 can prevent hydrogen atoms generated during fabrication or included in carrier gas from permeating the ferroelectric layer pattern 50. If hydrogen atoms permeate the ferroelectric layer pattern 50 they reduce the reliability of the ferroelectric layer pattern 50 by reacting to oxygen atoms inside the ferroelectric layer pattern 50 to produce oxygen vacancies, which degrade the polarization characteristics of the ferroelectric capacitor. Consequently, this leads to the malfunction of the ferroelectric memory device.

In addition, if hydrogen atoms spread in the interface between the ferroelectric layer pattern 50, the upper electrode 55 and the lower electrode 45, the energy barrier between them is lowered degrading the leakage current characteristics of the ferroelectric capacitor. As a result, the encapsulated barrier layer 90 improves the characteristics and reliability of the ferroelectric capacitor 60.

The via etch blocking layer pattern 80 is covered by the upper interlayer insulating layer. It is preferable that the via etch blocking layer pattern 80 and the upper interlayer insulating layer are made of materials with a different etch selectivity. For example, if the upper interlayer insulating layer is made of an oxide layer, the via etch blocking layer pattern is made of a titanium oxide layer, a silicon nitride layer or a silicon oxynitride layer. The upper interlayer insulating layer includes the $1^{st}$ upper interlayer insulating layer 95 and the $2^{nd}$ upper interlayer insulating layer 110. A plurality of main word lines 105a are formed between the $1^{st}$ upper interlayer insulating layer 95 and the $2^{nd}$ upper interlayer insulating layer 110. The main word lines 105a control four gates 15 through a decoder.

A plurality of plate lines 120 are formed directly in contact with the ferroelectric capacitors 60 disposed on at least two neighboring lines through a slit-shaped common via hole passing through the 2nd upper interlayer insulating layer, the 1st upper interlayer insulating layer and the encapsulated barrier layer 90. These plate lines 120 contact the via etch blocking layer pattern 80 between the ferroelectric capacitors 60.

As described in detail, plate lines and capacitors are connected through a slit-shaped common via hole, removing elements which restrict integration in forming via holes for connection of plate lines in each cell. Therefore, such a ferroelectric memory device can be more highly integrated by improving the connecting structure with plate lines in a reduced capacitor according to reductions of the design rule.

Hereinafter, a method for fabricating a ferroelectric memory device according to an embodiment of the present invention is described. FIGS. 1 through 8 are cross-sectional views showing a method for fabricating a ferroelectric memory device according to the embodiment of the present invention in FIG. 9.

As shown in FIG. 1, a plurality of cell transistors are formed two-dimensionally on the semiconductor substrate 10 after an isolation process, in the line direction and in the column direction. After forming a plurality of gates, a source region 17 and a drain region 18 are formed on the semiconductor substrate 10 at both sides of each gate 15 by implanting impurities. A cell transistor includes the gate 15, the source region 17 and a drain region 18 at both sides of the gate 15. Next, the contact pad 25 is formed on the source region 17 and the drain region 18. The contact pad 25 can be formed of doped polycrystalline silicon and can be self-aligned.

After forming the 1st lower interlayer insulating layer 20 on the semiconductor substrate 10, on which the contact pad 25 is formed, a bit line 30 is formed to be electrically connected to the drain region 18 of the cell transistor by passing through the 1st lower interlayer insulating layer 20 by the contact pad 25.

After forming the 2nd lower interlayer insulating layer 35 on the semiconductor substrate 10, on which the bit line 30 is formed, a plurality of contact plugs 40 are formed to be electrically connected to the source region 17 of the cell transistor by passing through the 2nd lower interlayer insulating layer 35 and the 1st lower interlayer insulating layer 20 by the contact pad 25.

In addition, a lower electrode layer, a ferroelectric layer and an upper electrode layer are formed sequentially on top of the 2nd lower interlayer insulating

layer 35 including the contact plugs 40. The lower electrode layer can be formed of multiple layers including an adhesive layer, a lower diffusion barrier layer, a lower metallic oxide layer and a lower metallic layer and its total thickness can range between 1000 and 3000Å. It is noted that the lower diffusion barrier layer is formed to prevent oxygen from extending. The upper electrode layer can be a dual layer of an upper metallic oxide layer, and an upper diffusion barrier layer, and its total thickness can range from 1000 and 3000Å. The upper electrode and the lower electrode are made of a metal such as Pt, Ir, Ru, Rh etc. and their oxides. The ferroelectric layer is made of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer or $SrBi(Ta, Nb)_2O_9$ in Spin Coating, or by LSMCD (Liquid Source Mist Chemical Vapor Deposition), Chemical Vapor Deposition, or Physical Vapor Deposition.

A lower electrode layer, a ferroelectric layer and an upper electrode layer are patterned using a mask, to form a plurality of ferroelectric capacitors in which a lower electrode layer 45, a ferroelectric layer pattern 50 and an upper electrode 55 are layered sequentially. The ferroelectric capacitors 60 are formed on top of the contact plugs 40. Since the cell transistors are two-dimensionally disposed, therefore, the contact plugs 40 and the ferroelectric capacitors 60 are also two-dimensionally disposed.

It is not possible to etch using the existing three masks, because an overlay margin is considerably reduced in a highly integrated ferroelectric memory device. Instead, a capacitor node separation is performed by general photo etching using one hard mask layer made of a titanium nitride layer and a photoresist.

Next, as shown in FIG. 2, an interlayer insulating layer 70 covering the ferroelectric capacitor 60 is formed, on which a via etch blocking layer 80 is formed. The via etch blocking layer 80 is formed of a titanium oxide layer, a silicon nitride layer or a silicon oxynitride layer.

As shown in FIG. 3, the via etch blocking layer 80 and the interlayer insulating layer 70 are patterned in each cell, thereby forming cell via holes 85 exposing each upper electrode 55.

Next, as shown in FIG. 4, an encapsulated barrier layer 90 is clad along with the via etch blocking layer pattern 80 to prevent hydrogen from permeating. The encapsulated barrier layer 90 can be formed of an aluminium oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer or a cesium oxide layer.

Further, the encapsulated barrier layer 90 can prevent hydrogen atoms generated during fabrication or included in carrier gas from permeating the ferroelectric layer pattern 50. As described above, hydrogen atoms should be excluded from as much as possible. Basically, hydrogen diffuses into the ferroelectric capacitor layer pattern through the upper electrode, deoxidizing the oxidized substances in the ferroelectric substance. As a result, the ferroelectric characteristics are degraded and adhesion to the upper electrode of the ferroelectric layer pattern is decreased due to chemical changes at the interface. The upper electrode is elevated upwards by products such as oxygen, water which are produced in an oxidation-reduction reaction. The upper electrode and the ferroelectric layer pattern easily liftoff at the interface. Accordingly, hydrogen atoms are excluded by the encapsulated barrier layer 90.

Referring to FIG. 5, the via etch blocking layer pattern 80, which fills the cell via hole 85, is covered with the 1st upper interlayer insulating layer 95. It is preferable that the 1st upper interlayer insulating layer 95 is made of another substance with a different etch selectivity from the via etch blocking layer pattern 80. In the case that a titanium oxide layer, a silicon nitride layer or a silicon oxynitride layer is used as the via etch blocking layer pattern 80, an oxide layer can be used as the 1st upper interlayer insulating layer. The conductive layer 105 is formed on top of the 1st upper interlayer insulating layer 95. As the conductive layer 105, a layer made of metal such as aluminium can be used.

Referring to FIG. 6, the main word lines 105a are formed on top of the 1st upper interlayer insulating layer 95 by patterning a conductive layer 95. Generally, each of the main word lines 105a control four gates 15 through a decoder.

As shown in FIG. 7, the 2nd upper interlayer insulating layer 110 is formed on the resultant structure, on which the main word lines 105a are formed. If the main word lines 105a and their subsequently formed plate lines are made of metal, the 2nd upper interlayer insulating layer 110 is an intermetal insulating layer.

Subsequently, a slit-shaped common via hole 115 which exposes the upper electrode 55 of the neighboring capacitor 60 is formed as shown in FIG. 8. As seen in the sectional view, the slit-shaped common via hole appears to expose the upper electrodes of only two capacitors, but more upper electrodes are exposed as can be seen in the plane views. It is preferable that the upper electrode 55 of the ferroelectric capacitors 60 on at least two lines are exposed. At this time, the 2nd

upper interlayer insulating layer 110 and the 1st upper interlayer insulating layer 95 are etched using the via etch blocking layer pattern 80 as an etch finish point. An encapsulated barrier layer 90, which is exposed in this process, is also etched. The via etch blocking layer pattern 80 protects the interlayer insulating layer 70 between the ferroelectric capacitors 60 from being etched, since the other substance which as a different etch selectivity is used as the via etch blocking layer pattern 80. Accordingly, etching chemicals do not permeate the ferroelectric layer pattern 50, so that capacitors are not degraded. In the regions without the via etch blocking layer pattern 80, the 2nd upper interlayer insulating layer 110 and the 1st upper interlayer insulating layer 95 are etched and then the upper electrode 55 of the capacitor is exposed.

Next, the plate lines 120 are formed by depositing a layer of metal such as aluminium, completing the fabrication of a ferroelectric memory device as shown in FIG. 9. The plate lines 120 are electrically connected to the ferroelectric capacitors 60 disposed on at least two neighboring lines, and contact the via etch blocking layer pattern 80 between the ferroelectric capacitors 60.

As described above, when a slit-shaped via hole is formed using the via etch blocking layer as an etch finishing point according to an embodiment of the present invention, the lower interlayer insulating layer is not damaged. This overcomes the conventional problem where etching chemicals permeate the capacitor dielectric layer and degrade the capacitor characteristics.

It is noted that the present invention is not limited to the preferred embodiment described above, and it is apparent that variations and modifications can be made by those skilled in the art. For example, each of the plate lines can be connected to the capacitors on at least three neighboring lines.

[Effect of the Invention]

As described above, plate lines and capacitors are connected through a slit-shaped common via hole according to the present invention, aiding integration in forming via holes for connection of plate lines in each cell. In an embodiment of the present invention, a plate line directly contact the upper electrodes of the ferroelectric capacitors on at least two neighboring lines in a cell array. Accordingly, it is noted that integration of the ferroelectric memory device is considerably increased by the possession of the plate lines. In addition, the reliability of the ferroelectric memory device is greatly improved.

Further, since a via etch blocking layer is used as an etch finish point, the lower interlayer insulating layer is not damaged. This overcomes the conventional problem where etching chemicals permeate the capacitor dielectric layer and degrade the capacitor characteristics, and a very stable capacitor with highly improved characteristics can be fabricated by this process.

What is claimed is:

1. A ferroelectric memory device comprising:

a lower interlayer insulating layer formed on a semiconductor substrate;

a plurality of ferroelectric capacitors disposed two-dimensionally on the lower interlayer insulating layer in the line direction and the column direction;

an interlayer insulating layer covering between the ferroelectric capacitors and exposing the tops of the ferroelectric capacitors;

a via etch blocking layer pattern formed only on the interlayer insulating layer;

an upper interlayer insulating layer formed on the via etch blocking layer pattern; and

a plurality of plate lines, each electrically connected to the ferroelectric capacitors on at least two neighboring lines contact the via etch blocking layer between the ferroelectric capacitors.

2. The ferroelectric memory device of claim 1, wherein the via etch blocking layer and the interlayer insulating layer are made of materials of different etch selectivity.

3. The ferroelectric memory device of claim 2, wherein the upper interlayer insulating layer is made of an oxide layer, and the via etch stop layer is made of a layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer and a silicon oxynitride layer.

4. The ferroelectric memory device of claim 1, further comprising an encapsulated barrier layer which is clad on the via etch blocking layer pattern and deters permeation of hydrogen.

5. The ferroelectric memory device of claim 4, wherein the encapsulated barrier layer is a metallic oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer and a cesium oxide layer.

6. The ferroelectric memory device of claim 1, wherein the ferroelectric capacitors include a lower electrode, a ferroelectric layer pattern and an upper

electrode layered sequentially, and the plate lines directly contact the upper electrodes on at least two neighboring lines.

7. The ferroelectric memory device of claim 6, wherein the plate lines are common plate lines which directly contact the upper electrodes on at least two neighboring lines through a slit-shaped common via hole passing through the upper interlayer insulating layer.

8. The ferroelectric memory device of claim 6, wherein the ferroelectric layer pattern is one selected from the group consisting of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer and $SrBi(Ta, Nb)_2O_9$.

9. The ferroelectric memory device of claim 1, wherein the lower interlayer insulating layer comprises:

a plurality of cell transistors disposed two-dimensionally on the semiconductor substrate in the line direction and in the column direction;

a plurality of bit lines electrically connected to drain regions of the cell transistors; and

a plurality of contact plugs electrically connected to source regions of the cell transistors;

wherein the ferroelectric capacitors electrically contact source regions through the contact plugs.

10. The ferroelectric memory device of claim 7, wherein the upper interlayer insulating layer comprises:

a $1^{st}$ upper interlayer insulating layer and a $2^{nd}$ upper interlayer insulating layer, which are layered sequentially; and

main wordlines on both sides of the slit-shaped common via hole, between the $1^{st}$ upper interlayer insulating layer and the $2^{nd}$ upper interlayer insulating layer.

11. A method for fabricating a ferroelectric memory device comprising:

forming a lower interlayer insulating layer on a semiconductor substrate;

forming a plurality of ferroelectric capacitors two-dimensionally on the lower interlayer insulating layer, in the line direction and the column direction;

sequentially forming an interlayer insulating layer covering the ferroelectric capacitors and a via etch blocking layer;

patterning the via etch blocking layer and the interlayer insulating layer to form cell via holes which cover the ferroelectric capacitors and expose the tops of the ferroelectric capacitors;

forming a 1st upper interlayer insulating layer completely filling the cell via holes;

forming main wordlines on a top of the 1st upper interlayer insulating layer;

forming a 2nd upper interlayer insulating layer entirely covering the main wordlines; and

forming a plurality of plate lines to each electrically access the ferroelectric capacitors on at least two neighboring lines and contact the via etch blocking layer pattern between the ferroelectric capacitors, by etching the 2nd upper interlayer insulating layer and the 1st upper interlayer insulating layer using the patterned via etch blocking layer as an etch finishing point and depositing a conductive layer.

12. The method of claim 11, wherein the via etch blocking layer and the interlayer insulating layer are made of materials of different etch selectivity.

13. The method of claim 12, wherein the 1st upper interlayer insulating layer is made of an oxide layer, and the via etch blocking layer is made of a layer selected from the group consisting of a titanium oxide layer, a silicon nitride layer and a silicon oxynitride layer.

14. The method of claim 11, further comprising forming an encapsulated barrier layer to deter permeation of hydrogen, after patterning the via etch blocking layer and the interlayer insulating layer.

15. The method of claim 14, wherein the encapsulated barrier layer is made of a metallic oxide layer selected from the group consisting of an aluminum oxide layer, a titanium oxide layer, a zirconium oxide layer, a tantalum oxide layer and a cesium oxide layer.

16. The method of claim 11, wherein forming the ferroelectric capacitors comprises:

sequentially forming a lower electrode layer, a ferroelectric layer and an upper electrode layer on the lower interlayer insulating layer; and

patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer continuously to form a plurality of ferroelectric layers in which the lower electrode, the ferroelectric layer pattern and the upper electrode are layered sequentially.

17. The method of claim 11, wherein the plate lines directly contact the ferroelectric capacitors on at least the two neighboring lines, through a slit-shaped common via hole penetrating the 1st and 2nd interlayer insulating layers.

18. The method of claim 14, wherein the plate lines are common plate lines which directly contact the ferroelectric capacitors on at least two neighboring lines, through a slit-shaped common via hole permeating the 1st interlayer insulating layer, the 2nd interlayer insulating layer, and the encapsulated barrier layer.

19. The method of claim 16, wherein the ferroelectric layer is made of a layer selected from the group consisting of a $Pb(Zr, Ti)O_3$ layer, a $SrBi_2Ta_2O_9$ layer and $SrBi(Ta, Nb)_2O_9$.

20. The method of claim 11, further, before forming the lower interlayer insulating layer, comprising:

forming a plurality of cell transistors two-dimensionally on the substrate of the semiconductor in a line direction and a column direction;

forming a 1st lower interlayer insulating layer on the semiconductor substrate having the plurality of cell transistors;

forming a plurality of bit lines electrically connected to the drain regions of the cell transistors through the 1st lower interlayer insulating layer;

forming a 2nd lower interlayer insulating layer on the entire surface of the semiconductor with the bit lines; and

forming a plurality of contact plugs which electrically connect the ferroelectric capacitor and the source regions of the cell transistors through the 2nd lower interlayer insulating layer and the 1st lower interlayer insulating layer.

FIG. 1

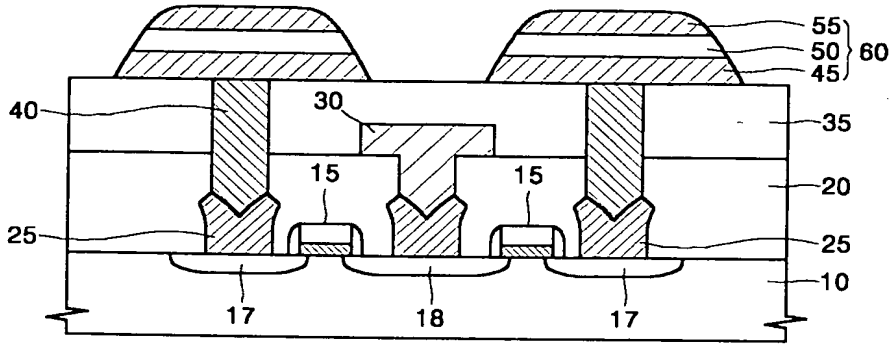


FIG. 2

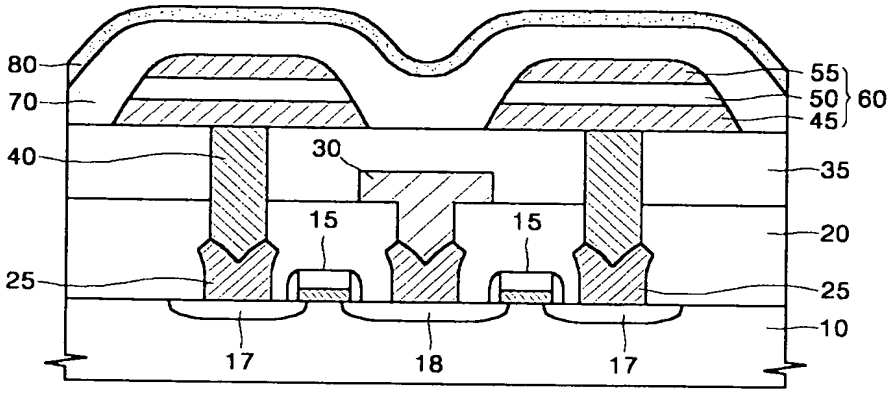

FIG. 3

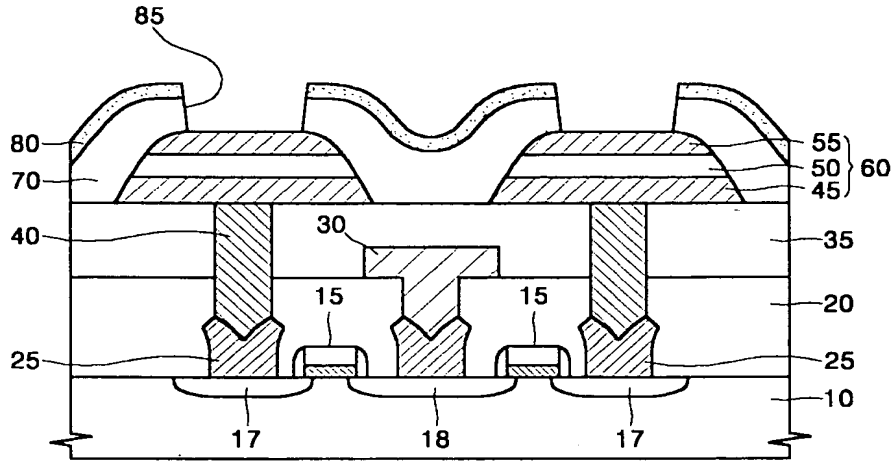
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FIG. 4

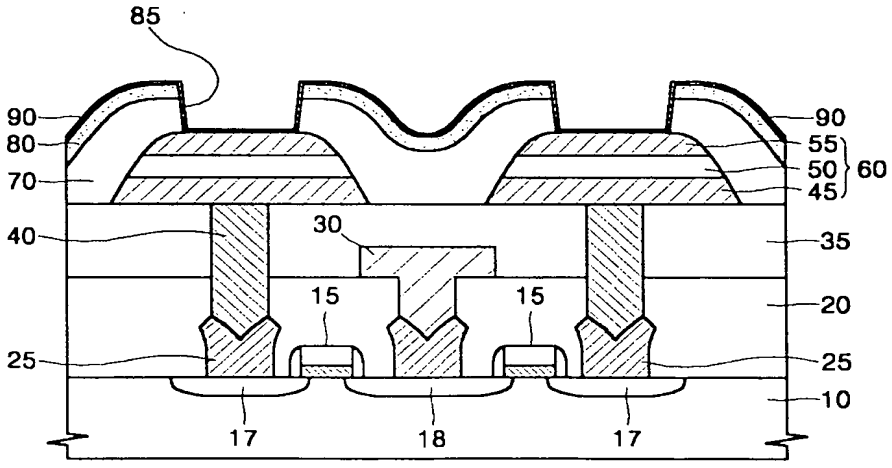
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FIG. 5

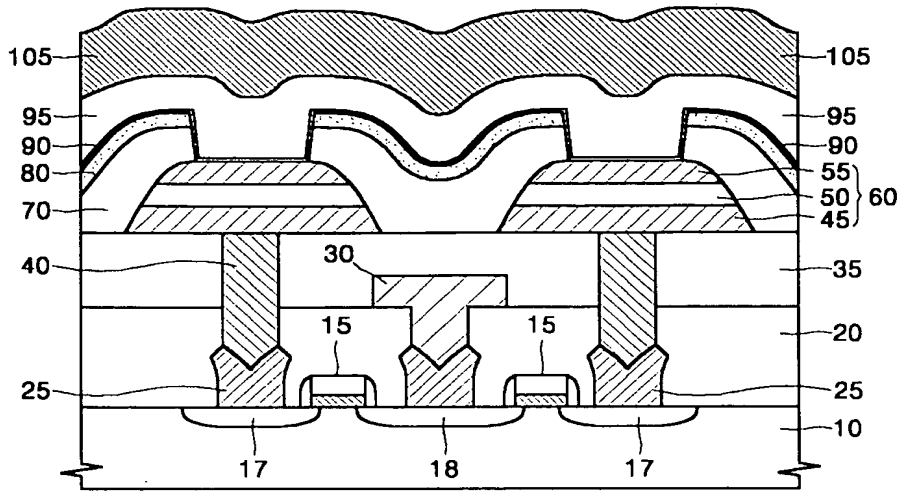
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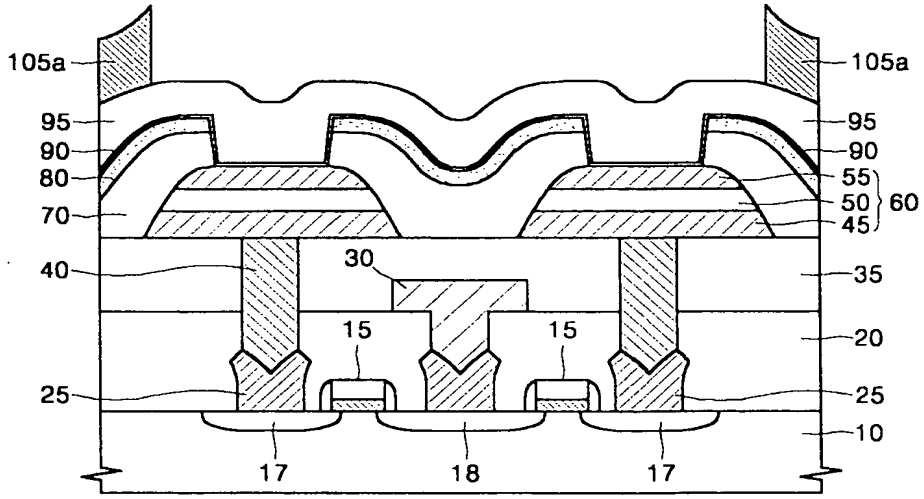
FIG. 6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17

FIG. 7

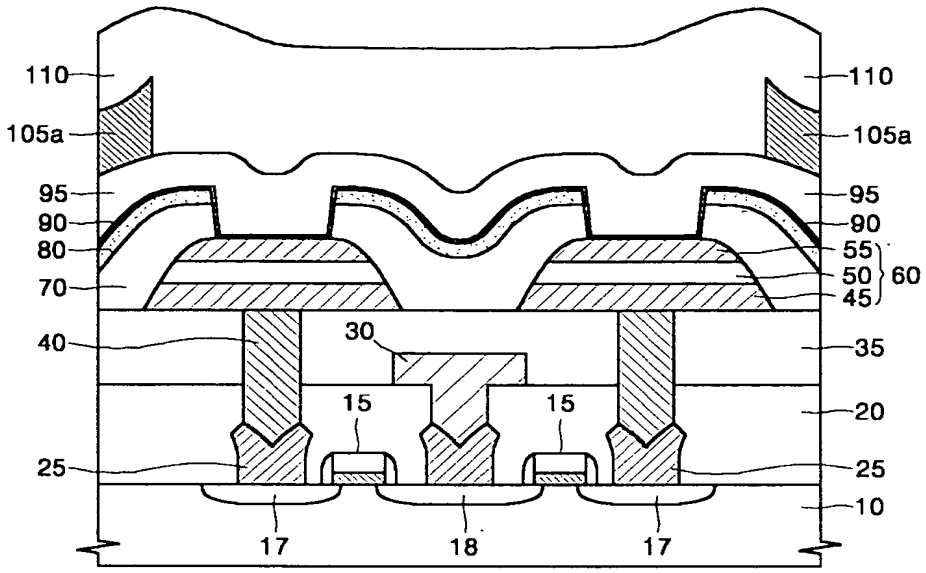
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FIG. 8

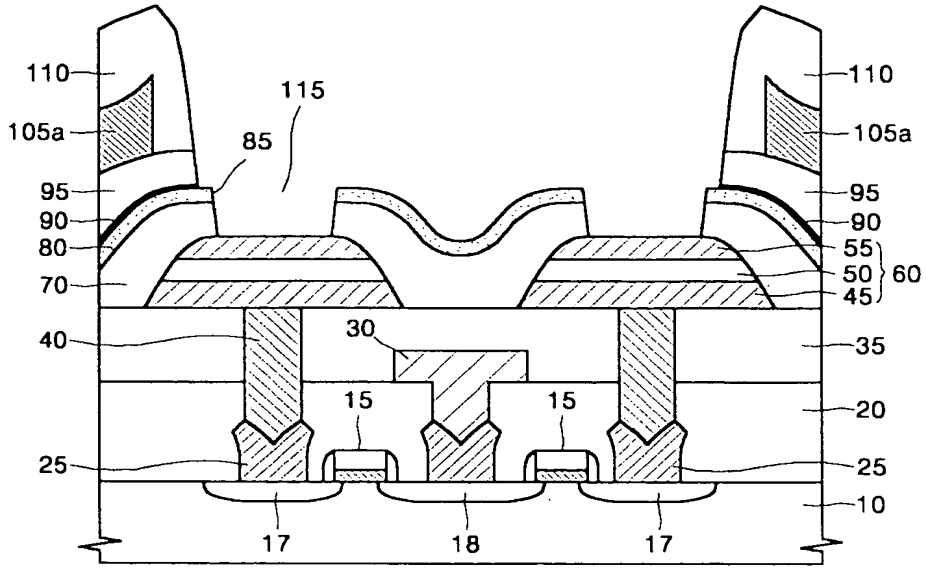
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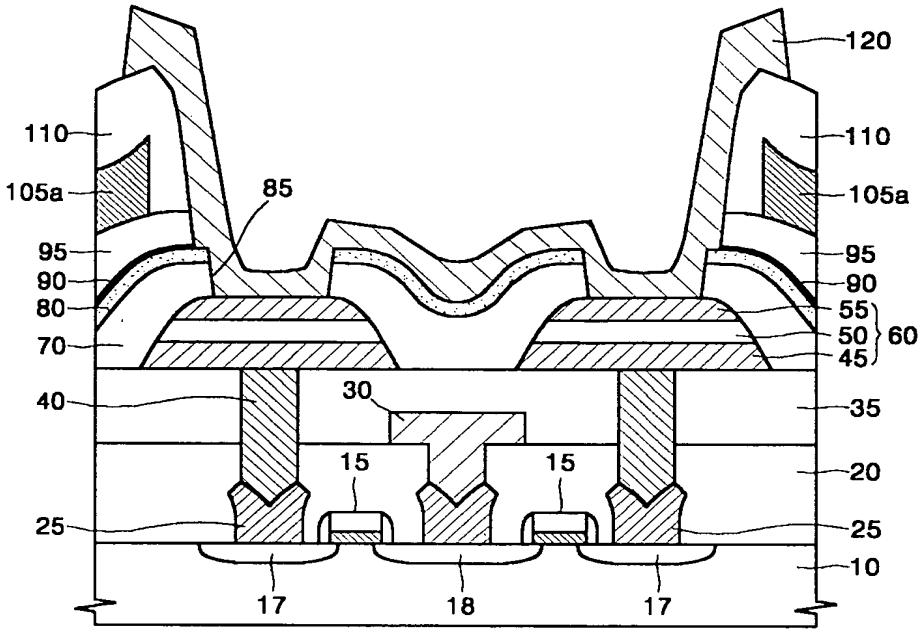
FIG. 9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